



Attorney's Docket No.: 10559-137001/P7876  
Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.      Art Unit: 2155  
Serial No.: 09/475,614      Examiner: David Y. Eng  
Filed : December 30, 1999  
Assignee : Intel Corporation  
Title : METHOD AND APPARATUS FOR CONTROL OF RECEIVE DATA

**Mail Stop Amendment**

Commissioner for Patents  
P.O. Box 1450  
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**OCT 25 2004**

**Technology Center 2100**

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Applicants call attention to the attached Information  
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Kindly accept this Information Disclosure Statement under  
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enclosed.

The documents are in the English language; hence no concise  
explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the  
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Applicant : Gilbert Wolrich et al.  
Serial No.: 09/475,614  
Filed : December 30, 1999

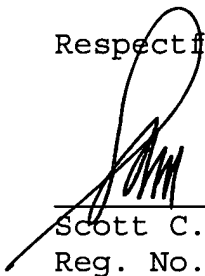
Attorney's Docket No.:10559-137001

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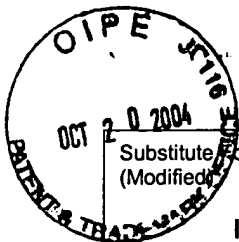
Respectfully submitted,

Date: October 18, 2004

  
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Substitute Form PTO-1449  
(Modified)U.S. Department of Commerce  
Patent and Trademark OfficeAttorney's Docket No.  
10559-137001Application No.  
09/475,614**Information Disclosure Statement  
by Applicant**

(Use several sheets if necessary)

(37 CFR §1.98(b))

Applicant  
Gilbert Wolrich et al.Filing Date  
December 30, 1999Group Art Unit  
2155**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/387,109	08/31/1999	Adiletta et al.			
	AB	09/473,571	12/28/1999	Wolrich et al.			
	AC	09/476,303	12/30/1999	Wolrich et al.			
	AD						
	AE						
	AF						

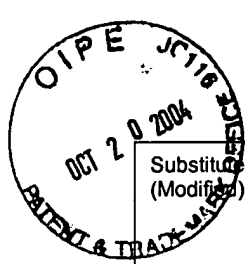
**RECEIVED****OCT 25 2004****Technology Center 2100****Foreign Patent Documents or Published Foreign Patent Applications**

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AG	0 379 709	08/01/1990	Europe				
	AH	0 464 715	01/08/1992	Europe				
	AI	0 633 678	01/11/1995	Europe				
	AJ	0 745 933	12/04/1996	Europe				
	AK	0 809 180	11/26/1997	Europe				
	AL	59-111533	06/27/1984	Japan				
	AM	WO 94/15287	07/07/1994	WIPO				
	AN	WO 97/38372	10/16/1997	WIPO				
	AO	WO 01/16782	03/08/2001	WIPO				
	AP	WO 01/16770	03/08/2001	WIPO				
	AQ	WO 01/16769	03/08/2001	WIPO				
	AR	WO 01/15718	03/08/2001	WIPO				
	AS	WO 01/48619	07/05/2001	WIPO				
	AT	WO 01/48606	07/05/2001	WIPO				
	AU	WO 01/48596	07/05/2001	WIPO				
	AV	WO 01/50679	07/12/2001	WIPO				
	AW	WO 01/50247	07/12/2001	WIPO				
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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-137001	Application No. 09/475,614
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date December 30, 1999	Group Art Unit 2155

**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AY	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AZ	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 <sup>nd</sup> ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.
	AAA	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	ABB	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	ACC	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	ADD	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	AEE	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
	AFF	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	AGG	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998.
	AHH	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	AII	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 <sup>th</sup> Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AJJ	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998.
	AKK	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999.
	ALL	Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359.
	AMM	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.
	ANN	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	